UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,065	01/29/2004	Toshiharu Furukawa	ROC920030268US1	5663

30206 7590 12/07/2009

IBM CORPORATION
ROCHESTER IP LAW DEPT. 917
3605 HIGHWAY 52 NORTH
ROCHESTER, MN 55901-7829

EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
12/07/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

rociplaw@us.ibm.com

Office Action Summary	Application No.	Applicant(s)	
	10/767,065	FURUKAWA ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8 and 25-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8 and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/01/09, 11/10/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitation of “the semiconductor device”, as recited in claim 1, is unclear as to the structural relationship between the semiconductor device and the claimed transistor device structure.

The claimed limitations of “the source” and “the drain”, as recited in claims 2, 5 and 3, 4, respectively, are unclear as to the structural relationship between the “the source” and the “the drain”, and the claimed transistor device structure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 and 8, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (6,566,704).

Regarding claim 1, Choi et al. teach in figure 3F and related text a vertical transistor device structure formed on a substrate 200, the substrate 200 defining a substantially horizontal plane, the semiconductor device structure comprising:

a source region 40;

a drain region 50;

a gate electrode 20 disposed on the substrate, said gate electrode positioned vertically between said source region and drain region; and

a nanotube 100 including a first end physically and electrically coupled with said source region, a second end electrically coupled with said drain region, and a channel region extending vertically through said gate electrode between said source region and said drain region, and

said gate electrode configured to receive a control voltage effective to regulate current flow through said channel region between said source region and said drain region.

Choi et al. do not explicitly state in the embodiment of figure 3F a plurality of semiconducting nanotubes.

Choi et al. teach using a plurality of semiconducting nanotubes in the disclosed invention of a nano sized transistor (see, for example, column 3, lines 39-43), wherein figures 1-3 depict only a unit cell of the transistor (column 3, lines 41-43).

Choi et al. further teach in the embodiment of figure 4B connecting the plurality of semiconducting nanotubes 100 with a single drain region 50 and a single source region 40.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a plurality of unit cells of the transistor in Choi et al.'s device, such that a plurality of semiconducting nanotubes are present in the device, and to connect the plurality of semiconducting nanotubes with a single drain region and a single source region, in order to use the device in a practical application which requires a plurality of semiconducting nanotubes, such as a nano sized transistor, and in order to simplify the processing steps of making the device and to simplify the operation of the device, respectively.

Regarding claims 4-6 and 8, Choi et al. teach in figure 1 and related text an insulating layer 30 disposed between said drain and said gate electrode for electrically isolating said drain from said gate electrode, an insulating layer 10 disposed between said source and said gate electrode for electrically isolating said source from said gate electrode, wherein said at least one semiconducting nanotube is composed of arranged carbon atoms, wherein said at least one semiconducting nanotube is oriented substantially perpendicular to said horizontal plane.

Regarding claims 2-3, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the source and drain of a catalyst material

effective for growing said at least one semiconducting nanotube in Choi et al.'s device in order to simplify the processing steps of making the device.

Note that the process limitations of forming the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube, would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Claim Rejections - 35 USC § 102/3

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

> applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 25-28 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kim et al. (6,599,808).

Regarding claims 25-28, Kim et al. teach in figure 1 and related text a capacitor device structure 20 formed on a substrate (inherently therein, because the capacitor must be formed on some base), the capacitor device structure comprising:

an electrically conductive first plate 12 disposed on the substrate,

an electrically conductive second plate 22 disposed vertically above said first plate;

an electrically conductive layer 18 disposed between said first and second plates;

a plurality of nanotubes 10 having a first end electrically coupled with said first plate for increasing an effective area of said first plate and a second end, and each of said nanotubes extending vertically through said electrically conductive layer from said first plate toward said second plate; and

a dielectric layer having a first portion disposed between a respective one of said nanotubes and said electrically-conductive layer, and said dielectric layer having a second portion disposed between the respective one of said nanotubes and said

second plate such that the second portion separates the respective one of said nanotubes from said second plate,

wherein said at least one nanotube has a conducting molecular structure,

wherein said at least one nanotube has a semiconducting molecular structure, and wherein said dielectric layer comprises a shell that encases said at least one nanotube.

Regarding the claimed limitation of "each of said nanotubes extending vertically through said electrically conductive layer from said first plate toward said second plate", this feature is inherent in Kim et al.'s device, because the left and right edges of said electrically conductive layer 18 are located on both sides of each of said nanotubes 10 such that each of said nanotubes extends vertically through said electrically conductive layer from said first plate toward said second plate.

Regarding the claimed limitation of forming a plurality of dielectric layers, this is a process limitation which would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. Note that forming a plurality of dielectric layers of the same material versus forming one dielectric layer will result in two identical structures.

In the alternative, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form Kim et al.'s device on a substrate by using a plurality of dielectric layers, in order to have better stability for the device and in order to have better control over the isolation of the nanotubes, respectively.

Note that the combined device comprises “a plurality of dielectric layers, each of said plurality of dielectric layers having a first portion disposed between a respective one of said nanotubes and said electrically-conductive layer, and each of said plurality of dielectric layers having a second portion disposed between the respective one of said nanotubes and said second plate such that the second portion separates the respective one of said nanotubes from said second plate”, as claimed.

Response to Arguments

Applicant's arguments with respect to claims 1-6, 8 and 25-28 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
12/3/2009

/ORI NADAV/
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800